

Fig. 1

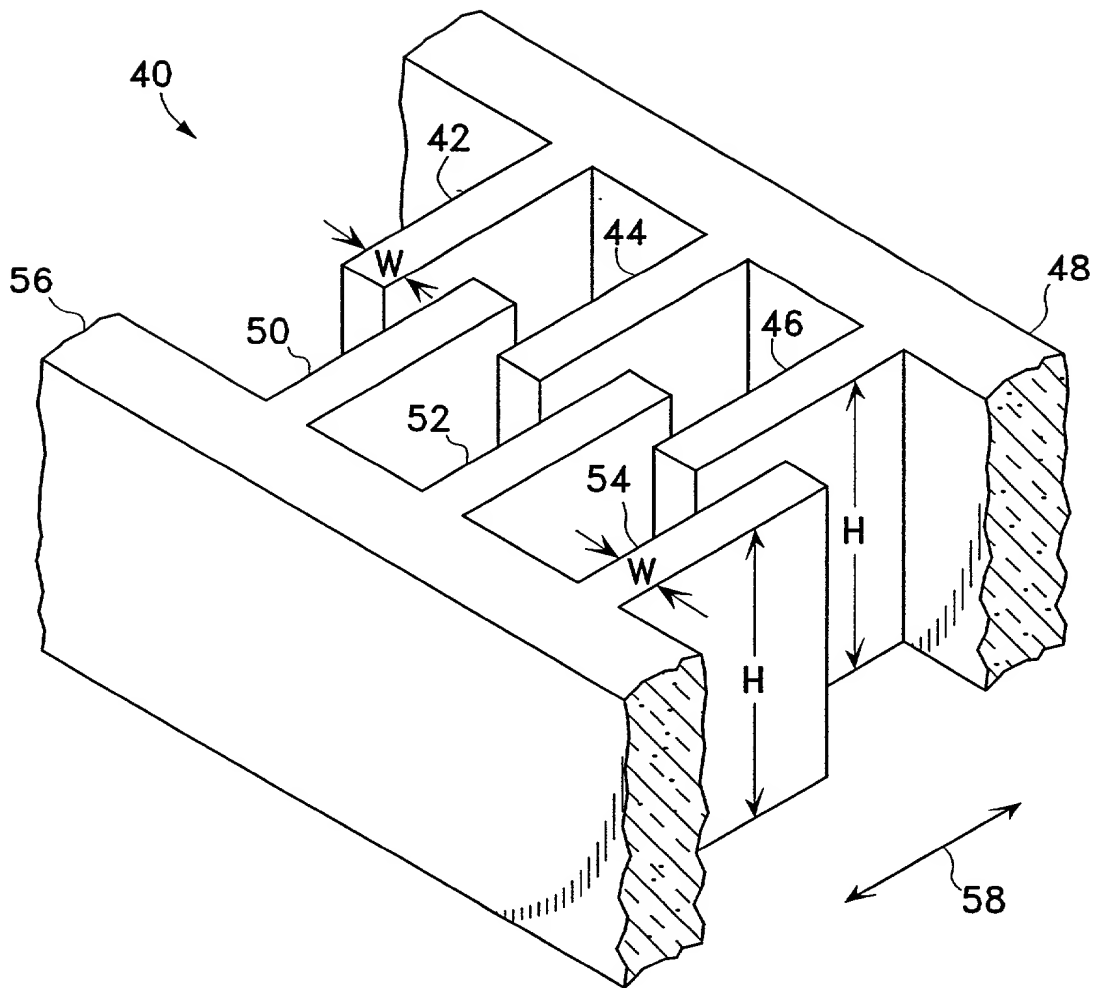


Fig. 2

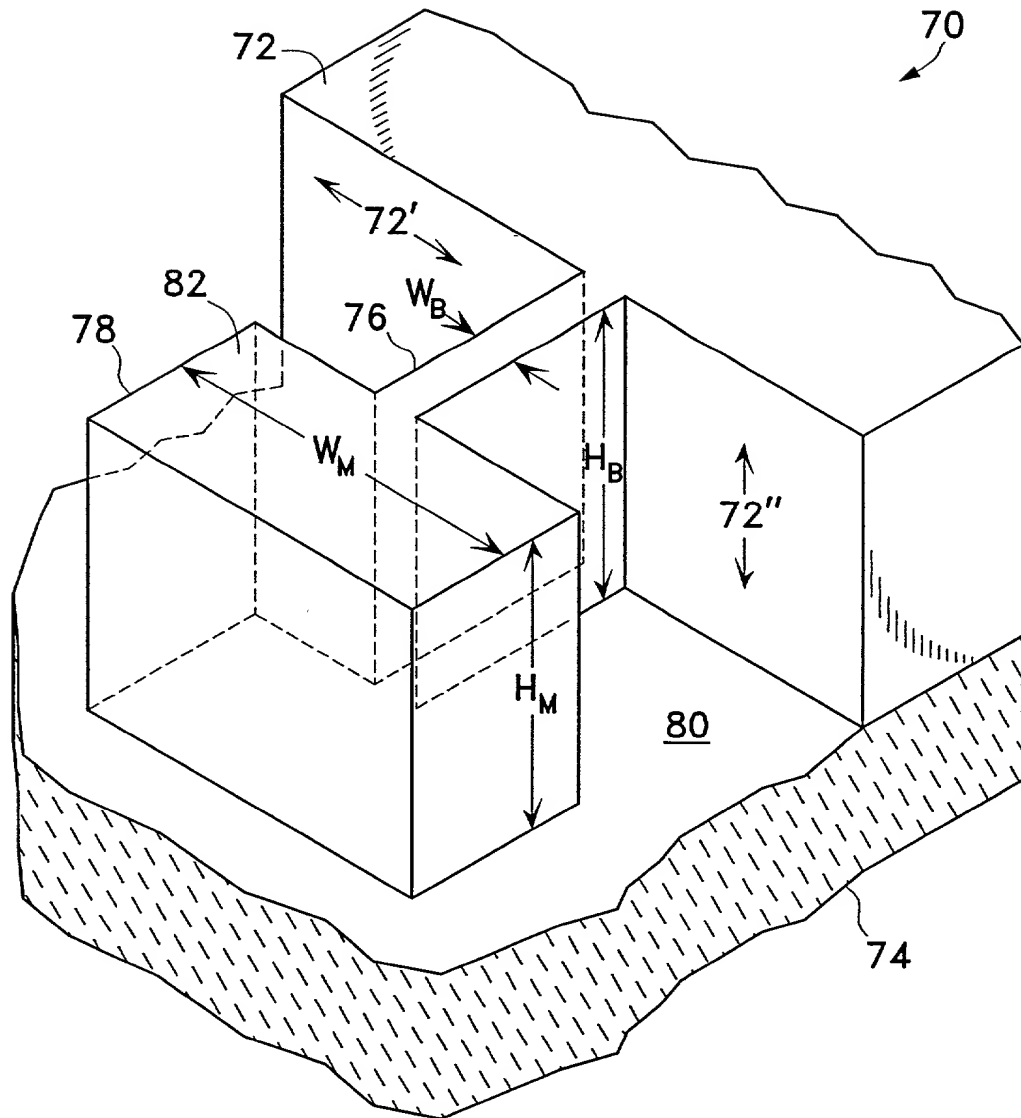


Fig. 3

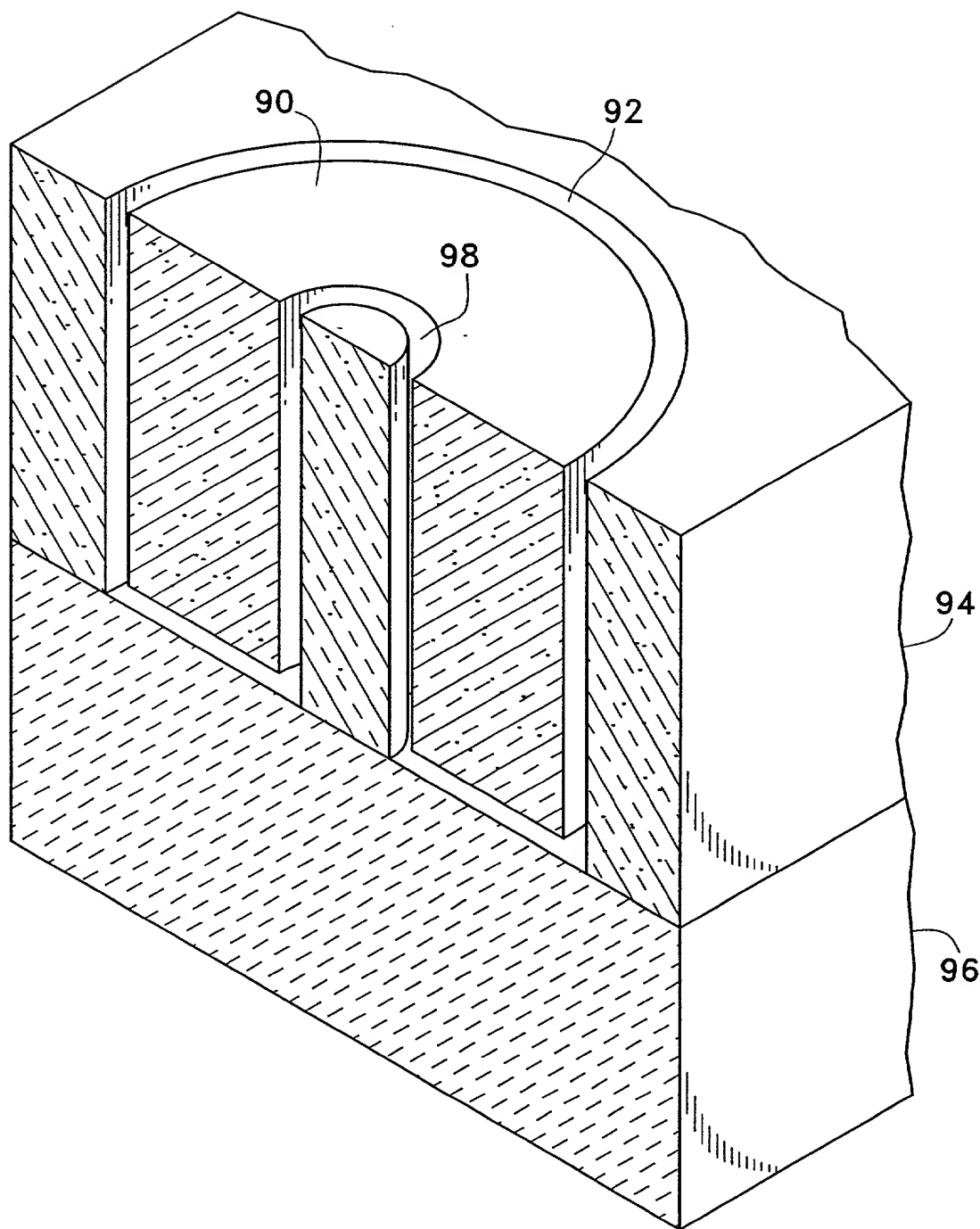
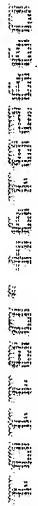


Fig. 4



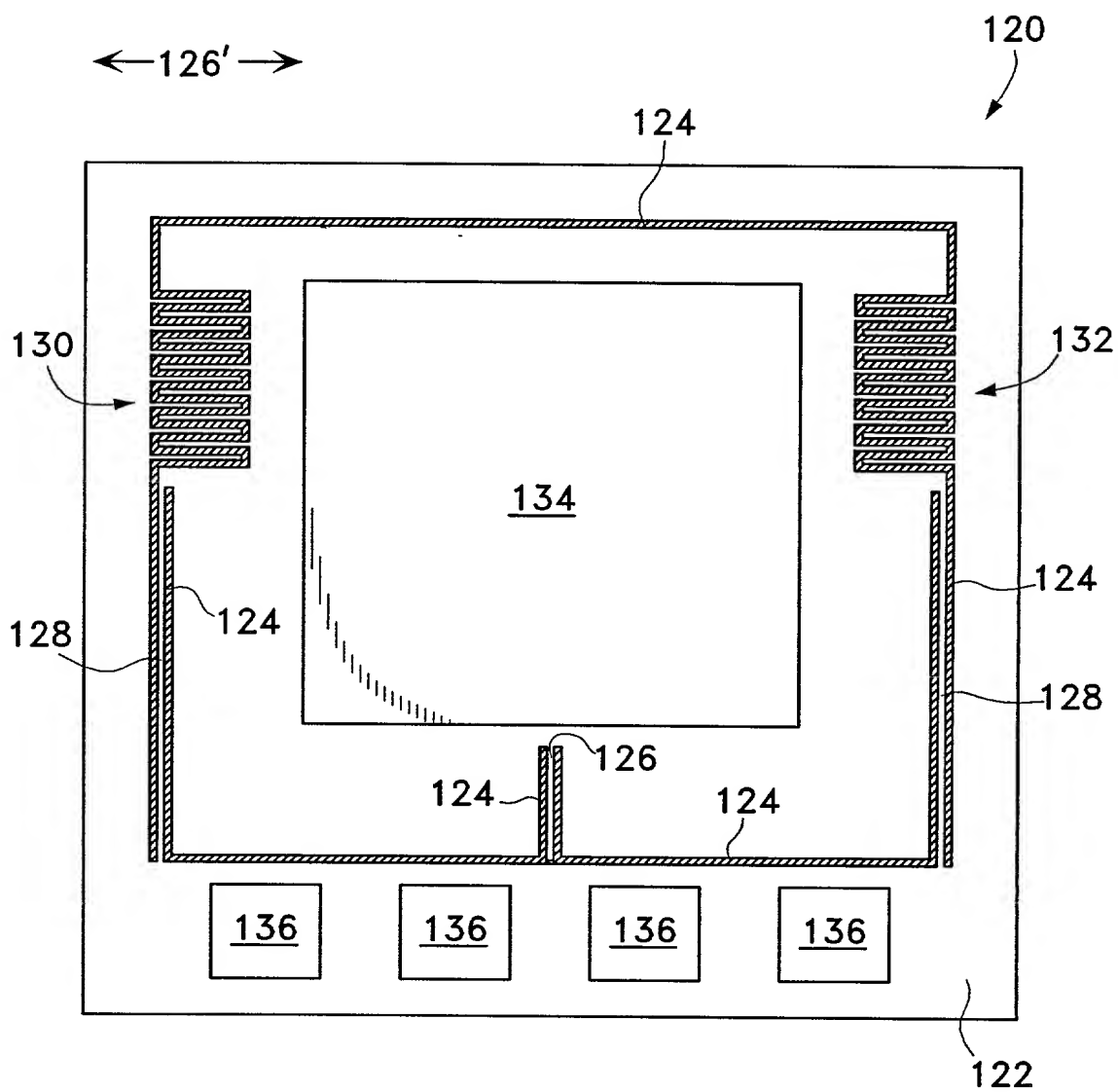


Fig. 6

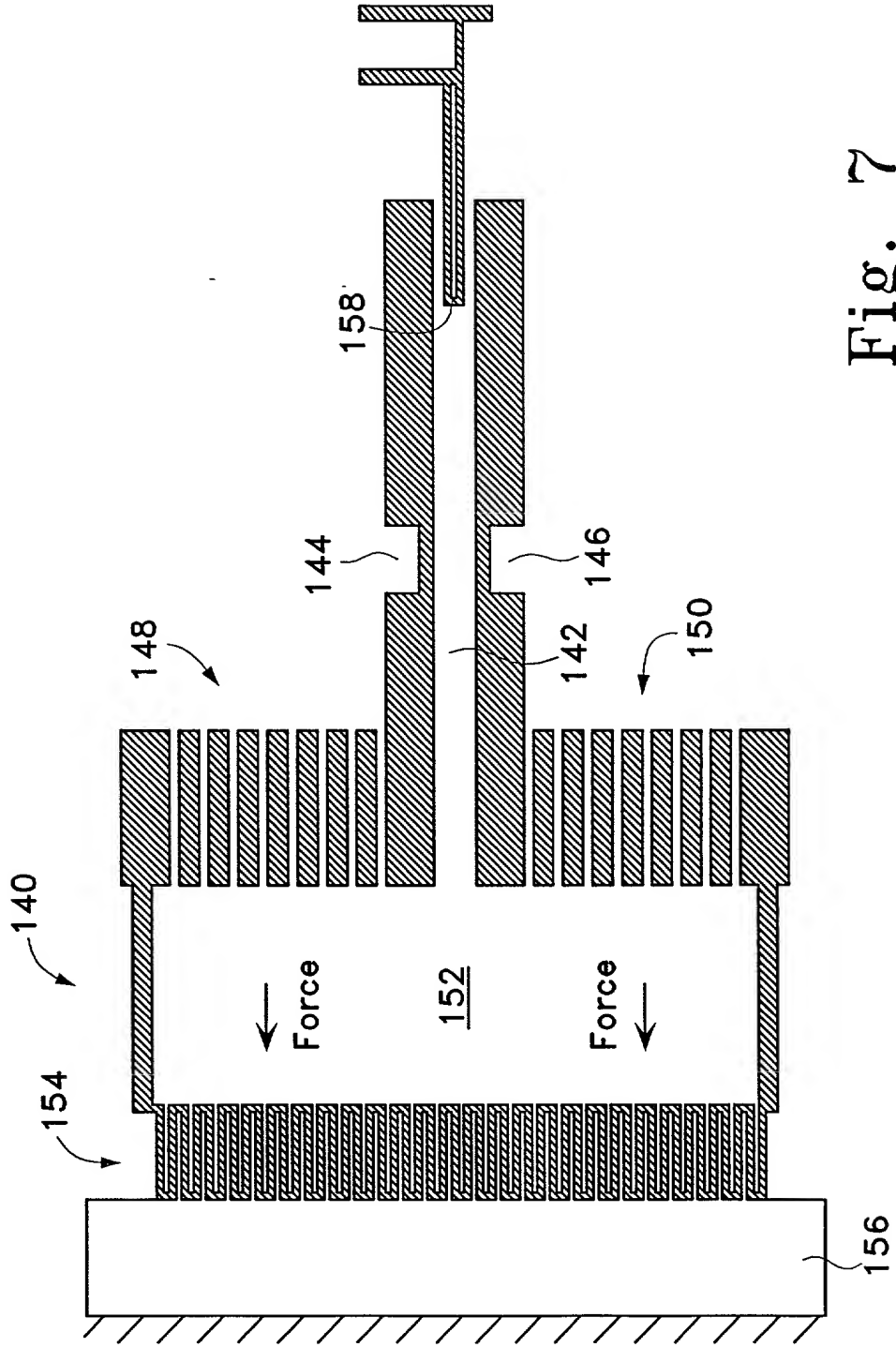


Fig. 7

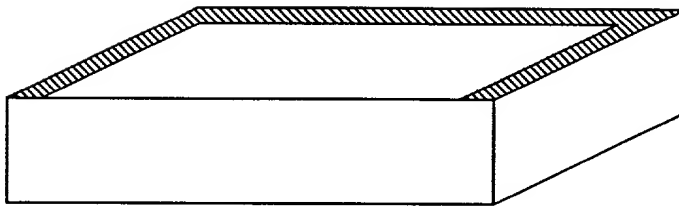


Fig. 8A

Pattern frontside with cavity mask and backside with alignment markers.

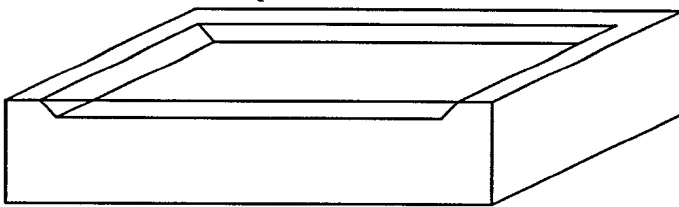


Fig. 8B

Timed anisotropic or plasma etch to form cavities.  
Strip frontside insulator.

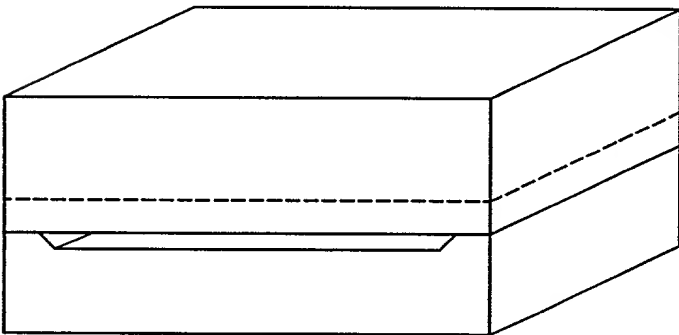


Fig. 8C

Silicon fusion band epi wafer to frontside. Epi thickness determines MEMS device thickness.

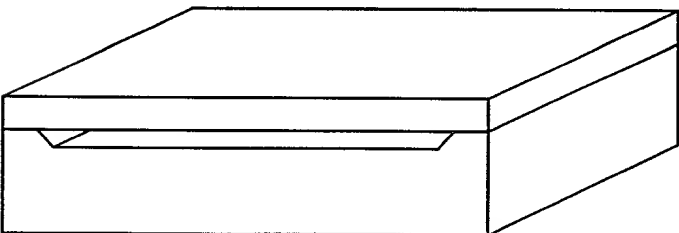


Fig. 8D

ECE etch to epi interface.

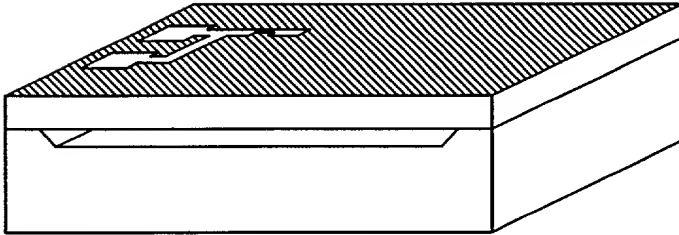


Fig. 8E

Deposit insulator on frontside and  
process sensing on chip circuits.

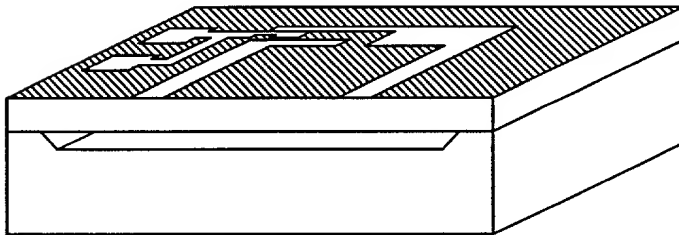


Fig. 8F

Define MEMS structure  
in insulator layer.

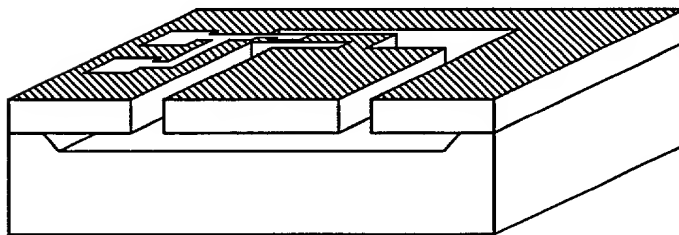


Fig. 8G

Anisotropic plasma etch  
to form MEMS structure.

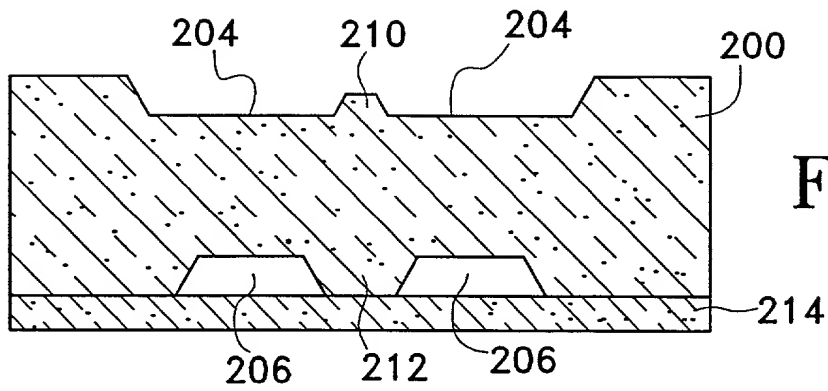


Fig. 9A

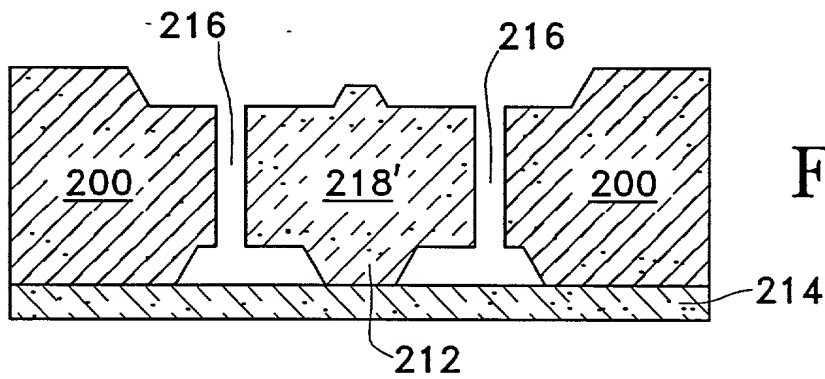


Fig. 9B

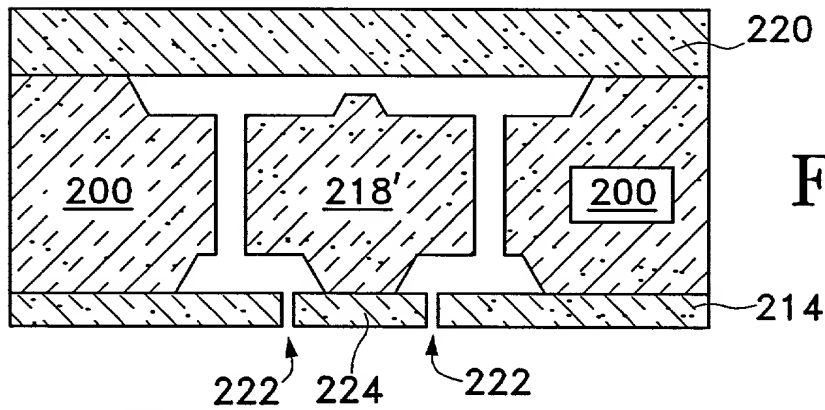


Fig. 9C

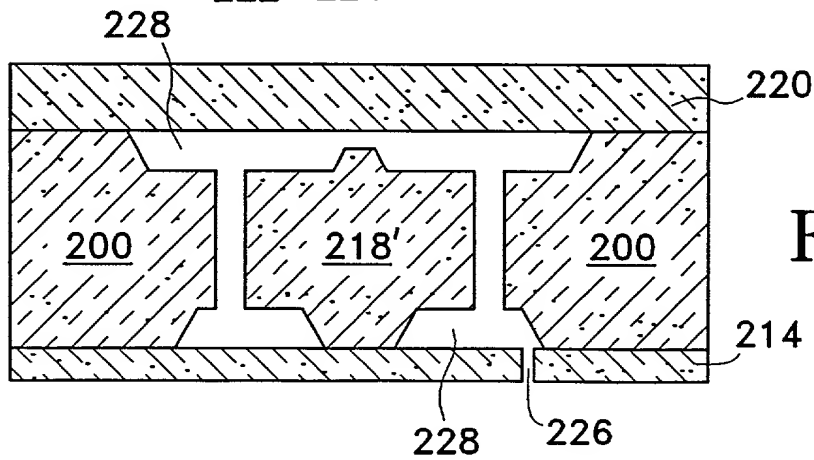


Fig. 9D

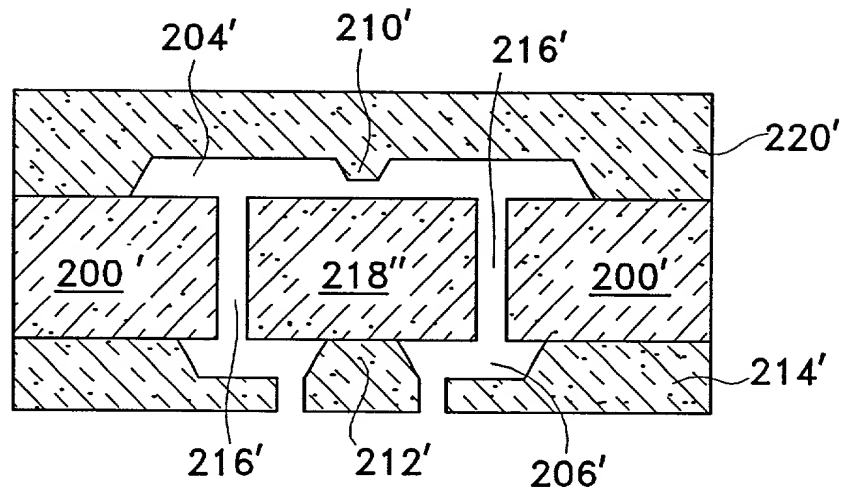


Fig. 10

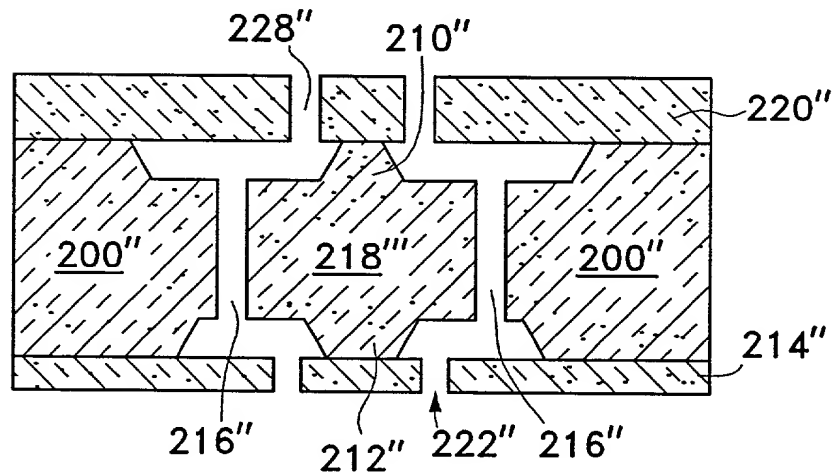
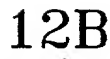


Fig. 11



12B



240

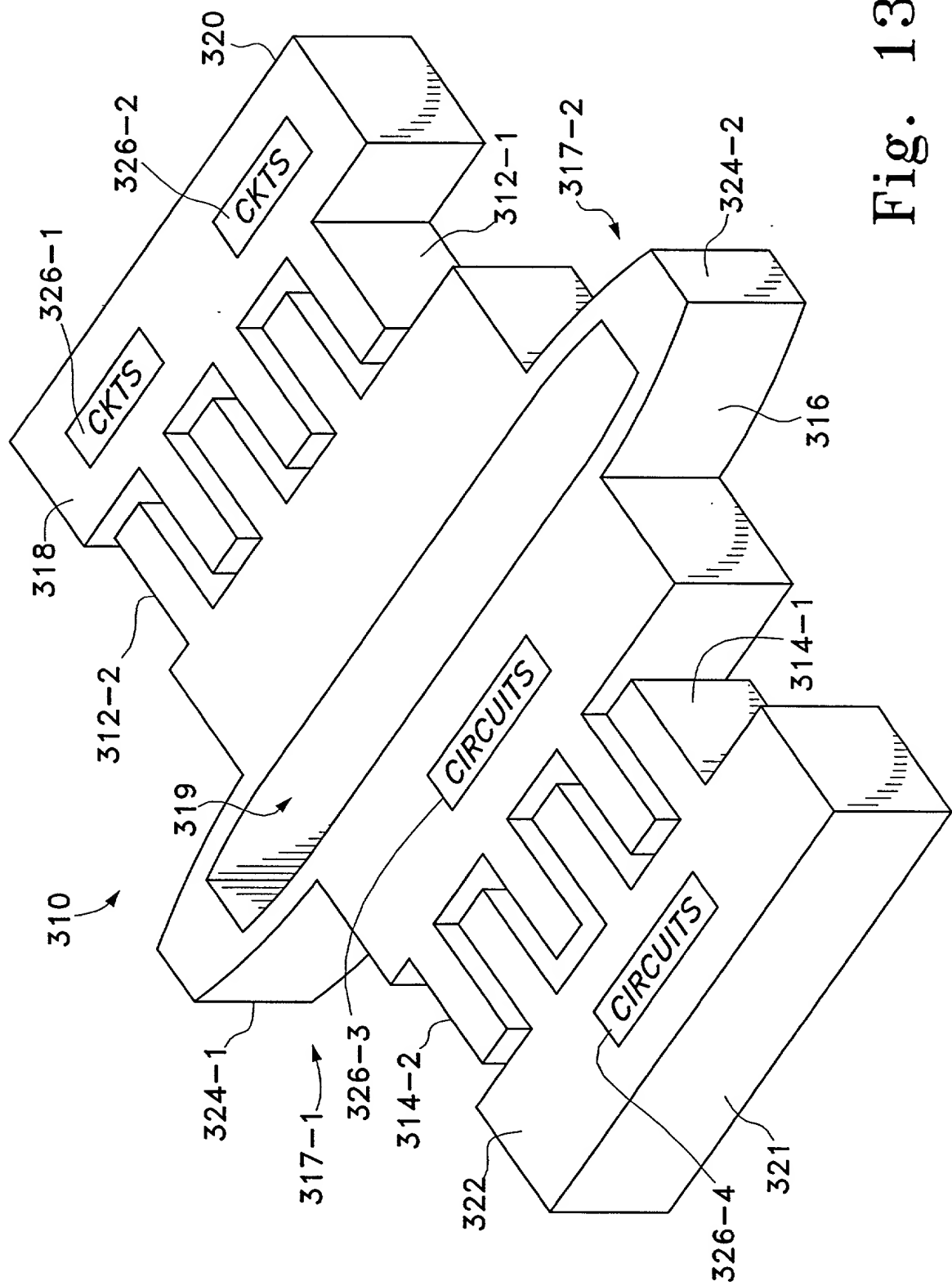


Fig. 13